ACCES I/O PRODUCTS, INC.
10623 Roselle Street, San Diego, CA 92121 • (858) 550-9559 • FAX (858) 550-7322
contactus@accesio.com • www.accesio.com

MODEL PCIe-DIO-24HC

Digital I/O Card

USER MANUAL

File PCIe-DIO-24HC.B1

Notice

The information in this document is provided for reference only. ACCES does not assume any liability arising out of the application or use of the information or products described herein. This document may contain or reference information and products protected by copyrights or patents and does not convey any license under the patent rights of ACCES, nor the rights of others.

IBM PC, PC/XT, and PC/AT are registered trademarks of the International Business Machines Corporation.

WARNING!!

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

Warranty

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations.

Terms and Conditions

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

Coverage

First Three Years: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

Equipment Not Manufactured by ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

General

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

Table of Contents

Chapter 1: Introduction

The PCIe-DIO-24HC is a x1 lane PCI Express (PCIe) board designed for use in a variety of Digital I/O (DIO) applications. It uses the high speed PCIe bus to transfer digital data to and from the board. The board includes a single 8255 chip and three 82C54 Counter/Timers making it easy to program. This also allows for simple migration from older ACCES' PCI-based DIO boards. IRQ capabilities relieve software from constant polling routines that consume valuable processing time. Lastly, the x1 lane PCIe connector is very flexible and can be inserted into any x1, x4, x8, x16, or x32 PCIe slots.

Features

- 24 high-current DIO lines
- Three 82C54 Counter/Timers
- IRQ generation from Port C bit 3, an external source & Counter A2, configurable for edge-(rising/falling) and/or level-triggered (high/low)
- DIO lines buffered
- Four and eight bit ports independently selectable for inputs or outputs
- Jumper selectable 10k ohm Pull-up/Pull-down resistors on DIO lines
- Jumper selectable VCCIO (5V, 3.3V)
- VCCIO voltage available to the user via 0.5A resettable fuse
- Latching 50 pin male header on card mounting bracket for secure cable retention

Applications

- Automatic Test Systems
- Laboratory Automation
- Robotics
- Machine Control
- Security Systems, Energy Management
- Relay Monitoring and Control
- Parallel Data Transfer to PC
- Sensing Switch Closures or TTL, DTL, CMOS Logic
- Driving Indicator Lights or Recorders

Functional Description

This product is a x1 lane PCIe DIO board with basic DIO, Counter/Timers and interrupt generation capabilities. The card uses an 8255 compatible chip, providing 24 DIO lines. The DIO lines are grouped into three 8-bit ports: A, B, and C. Each 8-bit port is configured via software to function as either inputs or outputs. Port C is further broken into two 4-bit nybbles via software, configured as either inputs or outputs.

Each DIO line is buffered and capable of up to 32mA source/sink. The VCCIO logic level is globally configured via jumper selection as 5V or 3.3V. Also, ports A, B, C low nybble, and C high nybble are individually jumper configurable as pull-up or pull-down through 10kΩ resistor networks.

There are three 82C54 counter(s) that each include three 16-bit counter/timers factory configured in an optimal mode for use as event counters, frequency output, pulse width, and frequency measurement.

The card is 4.824 inches in length and 4.2 inches seated height. I/O wiring for this board is via a right angle 50-pin latching male header connector. A ribbon cable can be used to connect this card to termination panels.

I/O wiring connections are via a 50-pin connector on the back plate of the card. Flat insulation-displacement ribbon cables can be used to connect these cards to termination panels and relay output cards. Also, the 50-pin connection provides compatibility with OPTO-22, Gordos, Potter & Brumfield and Western Reserve Controls module mounting racks. Fused VCCIO (5V or 3.3V via jumper selection) power is available on the I/O connector at pin 49. The on-board fuse is rated at 0.5A at room temperature, and can be reset by cycling computer power, or by removing the load.

The card can generate an interrupt to the computer on bit 3 of Port C if the IRQD jumper is installed and the INTSEL0 jumper is installed in the INT position. If the INTSEL0 jumper is installed on the EXT position, the interrupt will be generated by the external interrupt pin on the connector. The card also generates an interrupt to the computer on OUT2 of the first 82C54 if the IRQT jumper is installed. All interrupt trigger sources can be individually selected through software. When triggered, an interrupt is requested.

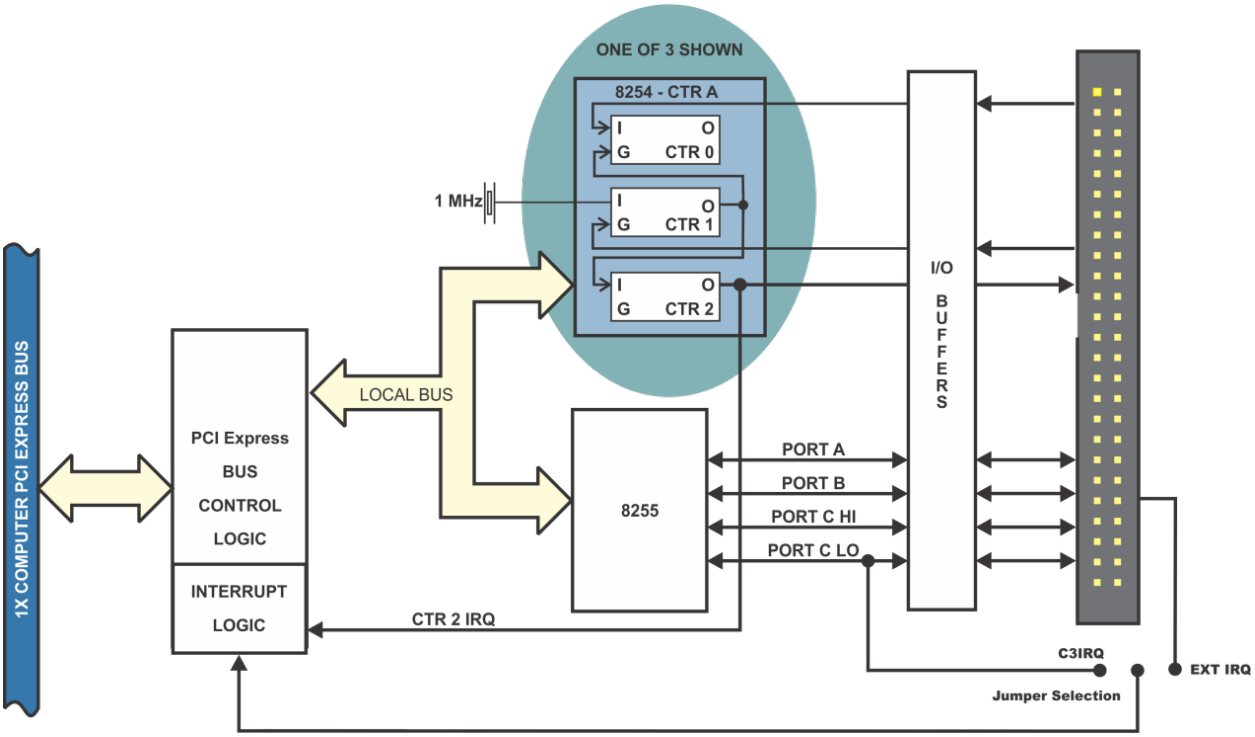


Figure 1-1: Block Diagram

Ordering Guide

- PCIe-DIO-24HC 24-bit Digital I/O card with three 8254's

Model Options

- -T Extended operating temperature (-40° to +85°C)

Included with your board

The following components are included with your shipment. Please take time now to ensure that no items are damaged or missing.

DIO Board
Packing Slip

Optional Accessories

CAB50F-6	CAB50-6	STB-120CH	ROB-24	1781-A24A
6 Foot Female to Female Ribbon Cable Assembly	6 Foot Female to Edge Card Ribbon Cable Assembly	Screw terminal boards installed in T-BOX	24 Electromechanical Relays Board	Solid State Module Mounting Rack w/Modules
				

Chapter 2: Installation

The software provided with this board is available by request on CD (see Optional Accessories in the ordering guide) for a fee, or downloaded via the product page for free and must be installed onto your hard disk prior to use.

Installing from Downloaded Installer

Windows

1. Visit the product web page at http://acces.io/cardname
2. Download the Software Package from the Downloads tab
3. Run the Install program and follow the on-screen prompts to install the software for this board

Linux

1. Please visit http://github.com/accesio for information on installing under Linux.

Caution! * ESD ***A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.***

Hardware Installation

Please install the software package before plugging the hardware into the system.

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETTINGS.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the blank back plate for an available PCIe slot. Carefully plug the card into the PCI Express expansion slot.
5. Inspect for proper fit of the card and tighten the bracket screw. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
6. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
7. Run one of the provided sample programs that was copied to the newly created card directory (from the CD or downloaded from the product page) to test and validate your installation.

Chapter 3: Hardware Details

Refer to the settings programs installed with the software package for the card. Also, refer to the Block Diagram and the Option Selection Map when reading this section of the manual.

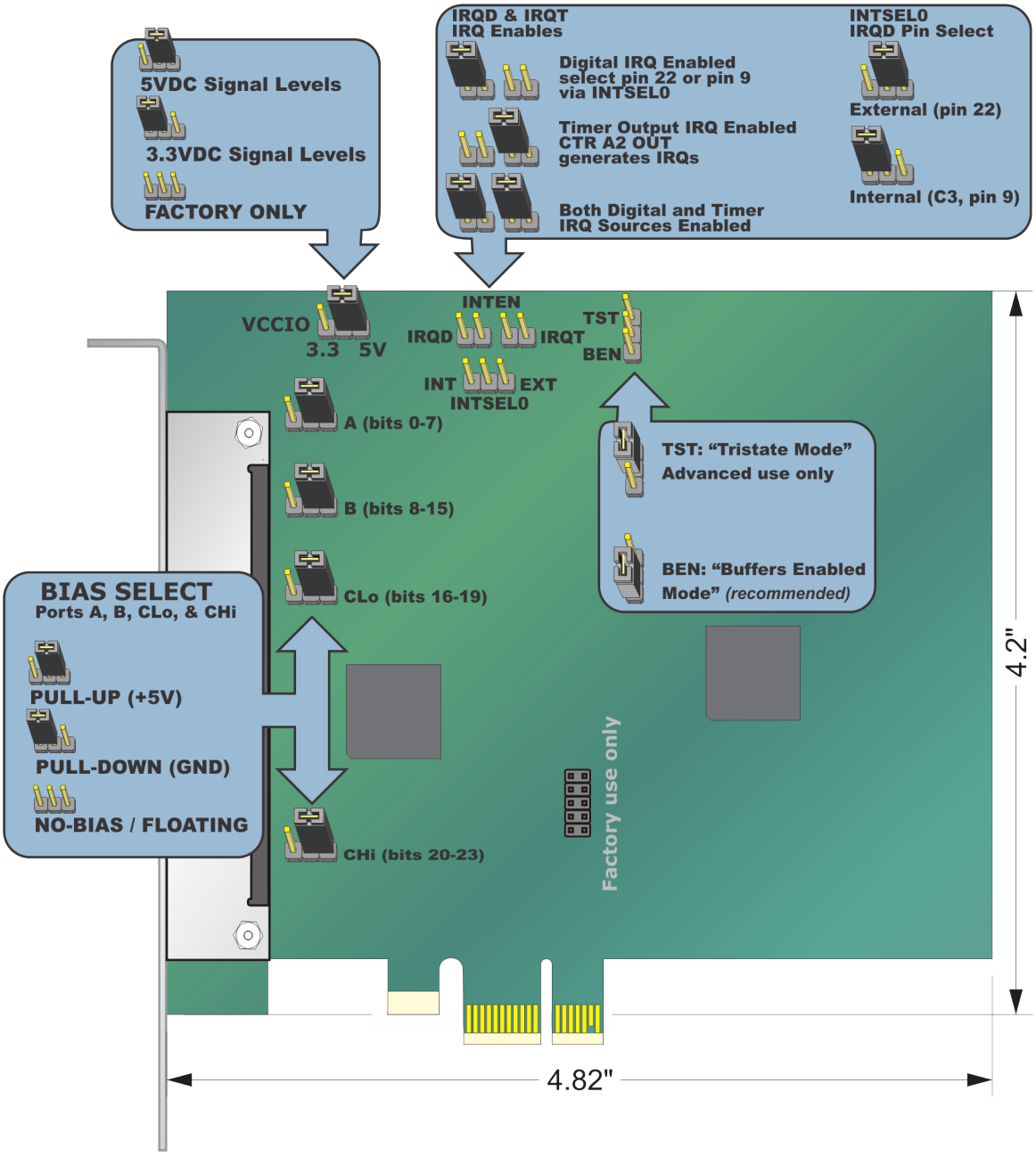


Figure 3-1: Option Selection Map

Buffer Mode Jumper

A means of enabling or disabling (tristating) the 74LVC8T245 input/output buffers under program control is provided at the jumper position labeled TST/BEN. When the jumper is in the BEN (Buffer Enable) position, the I/O buffers are always enabled. When the jumper is in the TST (Tristate) position, enabled/disabled state is controlled by a control register. See Chapter 5, Programming for a description.

Note
A jumper must be installed in EITHER the TST or the BEN position for the card to function.

Buffer VCCIO

VCCIO signaling levels are globally configured via jumper selection. Refer to the specifications chapter for signal levels for each possible selection.

Interrupt Mode Jumpers

Place the Interrupt Select 0 jumper in the INT position to select the Digital I/O interrupt (port C bit 3).
Place the Interrupt Select 0 jumper in the EXT position to select the External Input interrupt.

Install the IRQD jumper to enable the Digital I/O or External Input interrupts.
Install the IRQT jumper to enable the Timer generated interrupt.

The foregoing are the only manual setups necessary to use these cards. Input/Output selection is done via software by writing to a control register in the PPI as described in the Programming chapter of this manual.

Chapter 4: Address Selection

These cards use one address space, and occupy 22 register locations. These are defined in the Port Address Selection Table in the Programming section of this manual.

PCI Express architecture is inherently plug-and-play. This means that the BIOS or Operating System determines the resources assigned to PCI Express cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the AIOWDMFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI Express bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, some operating systems can be queried to determine which resources were assigned. In these operating systems, you can use either AIOWDMFind (Windows 7 or later) PCIFind or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for these cards is 494F. (ASCII for "IO")

The Device ID for the PCIe-DIO-24HC is 0C54.

Chapter 5: Programming

These cards are I/O-mapped devices that are easily configured from any language and any language can easily perform digital I/O through the card's ports. This is especially true if the form of the data is byte or word wide. All references to the I/O ports would be in absolute port addressing.

Developing Your Application Software

If you wish to gain a better understanding of the programs installed with the software package, then the information in the following paragraphs will be of interest to you.

A total of 22 register locations are used by this card

Address	Port Assignment	Operation
Base Address	PA Group 0	Read/Write
Base Address +1	PB Group 0	Read/Write
Base Address +2	PC Group 0	Read/Write
Base Address +3	Control byte	Write Only
Base Address +C	Enable/Disable Buffer	Write Only
Base Address +D	Disable Interrupts	Write Only
Base Address +E	Enable Interrupts	Write Only
Base Address +F	Clear Interrupt latch	Write Only
Base Address +10	Counter/Timer A0	Read/Write
Base Address +11	Counter/Timer A1	Read/Write
Base Address +12	Counter/Timer A2	Read/Write
Base Address +13	Counter/Timer A Control	Read/Write
Base Address +14	Counter/Timer B0	Read/Write
Base Address +15	Counter/Timer B1	Read/Write
Base Address +16	Counter/Timer B2	Read/Write
Base Address +17	Counter/Timer B Control	Read/Write
Base Address +18	Counter/Timer C0	Read/Write
Base Address +19	Counter/Timer C1	Read/Write
Base Address +1A	Counter/Timer C2	Read/Write
Base Address +1B	Counter/Timer C Control	Read/Write
Base Address +1C	Interrupt Enables	Read/Write
Base Address +1D	Interrupt Status	Read Only

Table 5-1: Address Assignment Table

8255

These cards use an 8255 PPI to provide a total of 24 bits input/output capability. The card is designed to use the PPI in Mode 0 wherein:

1. There are two 8-bit groups (A and B) and two 4-bit groups (C Hi and C Lo).
2. Any port can be configured as an input or an output.
3. Outputs are latched.
4. Inputs are not latched.

The PPI contains a Control Register. This write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. The PPI should be configured during initialization by writing to the Control Registers even if the ports are only going to be used as inputs. Output buffers are automatically set by hardware according to the Control Register states. Note that Control Register is located at base address +3 and bit assignments are as follows:

Bit	Assignment	Code
D0	Port C Lo (C0-C3)	1=Input, 0=Output
D1	Port B	1=Input, 0=Output
D2	Mode Select	1=Mode 1, 0=Mode 0
D3	Port C Hi (C4-C7)	1=Input, 0=Output
D4	Port A	1=Input, 0=Output
D5,D6	Mode Select	00=Mode 0, 01=Mode 1, 1X=Mode 2
D7	Mode Set Flag	1=Active

Table 5-2: Control Register Bit Assignment

Note

Mode 1 cannot be used by these cards without modification (Consult factory.). Thus, bits D2, D5, and D6 should always be set to "0". If your card has been modified for use in Mode 1, then there will be an Addenda sheet in the front of this manual. These cards cannot be used in PPI Mode 2 because of byte & nibble wide buffering .

Note

In Mode 0, do not use the control register byte for the individual bit control feature. The hardware uses the I/O bits to control buffer direction on this card. The control register should only be used for setting up input and output of the ports and enabling the buffer.

These cards provide a means to enable/disable the tristate I/O buffers under program control. If the TST/BEN jumper on the card is installed in the BEN position, the I/O buffers are permanently enabled. However, if that jumper is in the TST position, enable/disable of the buffers is software controlled via the control register as follows:

1. The card is initialized in the input mode by the computer reset command.
2. When bit D7 of the Control Register is set high, direction of the three groups of the associated PPI chip as well as the mode can be set. For example, a write to Base Address +3 with data bit D7 high programs port direction at 0 ports A, B, and C. If, for example, hex 80 is sent to Base Address +3, the Port 0 PPI will be configured in mode 0 with Groups A, B, and C as outputs. At the same time, data bit D7 is also latched in a buffer controller for the associated PPI chip. A high state disables the buffers and, thus, all four buffers will be put in the tristate mode; i.e. disabled.

3. Now, if any of the ports are to be set as outputs, you may set the values to that port with the outputs still in the tristate condition. (If all ports are to be set as inputs, this step is not necessary.)
4. If data bit D7 is low when the control byte is written, ONLY the associated buffer controller is addressed. If, for example, a control byte of hex 80 has been sent as previously described, and the data to be output are correct, and it is now desired to open the three groups, then it is necessary to send a control byte of hex 00 to base address +3 to enable the Port 0 buffers. When you do this, the buffers will be enabled.

Note

All data bits except D7 must be the same for the two control bytes

Those buffers will now remain enabled until another control byte with data bit D7 high is sent to base address +3.

Base Address +C (write) DIO Buffer Enable / Disable (tri-state)

At power-up or reset, all DIO buffers on the card are enabled. To globally disable the DIO buffers write a one to bit 7. To globally re-enable the DIO buffers, write a zero to bit 7. When the buffers are disabled the connector pins are tri-stated and biased by the state of the pull up or down configuration jumper.
Note, this is in addition to the tri-state control scheme at Base Address +3 bit 7; you can use either method interchangably.

Base Address +D (write) IRQ Disable Global

Write any value to this address to disable all IRQ sources on the card.

Base Address +E (write) IRQ Enable Global

Write any value to this address to enable all IRQ sources on the card as configured at +1C

Base Address +F (write) IRQ Clear

Any value written to this address will clear the status bit and pending IRQ.

Base Address +1C (read/write) Interrupt Enables

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQT Active Low	IRQT Active High	IRQT Falling Edge	IRQT Rising Edge	IRQD Active Low	IRQD Active High	IRQD Falling Edge	IRQD Rising Edge

Reading from this address will return the values last written. Writing a 1 to any bit will enable the corresponding function.
The card initializes with IRQD and IRQT rising edge enabled.

Base Address +1D (read) Interrupt Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Interrupt Status	IRQT Jumper Enable	IRQD Jumper Enable	Software Global IRQ (Base+D/E)	P2 pin 20 Digital Interrupt Disable

Reading from this address will return the status of each respective bit. A 1 signifies enabled, set and/or jumper installed. A 0 signifies disabled, cleared and/or jumper not installed.

8254 Counter/Timer

These cards have the option of one, two, or three 82C54 counter(s) that each include three 16-bit counter/timers factory configured in an optimal module for use as event counters, frequency output, pulse width, and frequency measurement (See Block Diagram). Each counter can be programmed to any count as low as 1 or 2, and up to 65,535, depending on the mode chosen. For those interested in more detailed information, a full description can be found in the Intel (or equivalent manufacturer's) data sheet.

Operational Modes

The 8254 modes of operation are described in the following paragraphs to familiarize you with the versatility and power of this device. For those interested in more detailed information, a full description of the 8254 programmable interval timer can be found in the Intel (or equivalent manufacturers') data sheets. The following conventions apply for use in describing operation of the 8254 :

Clock:	A positive pulse into the counter's clock input
Trigger:	A rising edge input to the counter's gate input
Counter Loading:	Programming a binary count into the counter

Mode 0: Pulse on Terminal Count

After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing.

Mode 1: Retriggerable One-Shot

The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. This forms a retriggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator

This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low. This mode also works well as an alternative to mode 0 for event counting.

Mode 3: Square Wave Generator

This mode operates like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency synthesis are two possible applications for this mode. Note that in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the wave form.

Mode 4: Software Triggered Strobe

This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter.

Mode 5: Hardware Triggered Strobe

In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

Counter/Timer Registers

Base + 10 Write/Read: Counter#A0 When writing, this register is used to load a count value into the counter. The transfer is either a single or double byte transfer, depending on the control byte written to the counter control register at BASE ADDRESS +13. If a double byte transfer is used, then the least-significant byte of the 16 bit value is written first, followed by the most significant byte. When reading, the current count of the counter is read. The type of transfer is also set by the control byte.

Base + 11 Write/Read: Counter #A1 See description for Base + 10 Write/Read.

Base + 12 Write/Read: Counter #A2 See description for Base + 10 Write/Read.

Base + 13 Write: Counter Control Register The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows: These cards contain a type 8254 programmable counter/timer that allows you to implement such functions as a Real Time Clock, Event Counter, Digital One-Shot, Programmable Rate Generator, Binary Rate Multiplier, Complex Wave Generator and/or a Motor Controller. The 8254 consists of three, 16-bit, presettable, down counters. Each counter can be programmed to any count between 1 or 2 and 65,535 in binary format depending on the mode chosen.

Programming the 8254

The counters are programmed by writing a control byte into the counter control register. Refer to the previous register map for the base addresses of the counters and the counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows:

B7	B6	B5	B4	B3	B2	B1	B0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0-SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter #0
0	1	Program Counter #1
1	0	Program Counter #2
1	1	Read/Write Cmd.*

* See section on Reading and Loading the Counters.

RW0-RW1: These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0-M2: These bits set the operational mode of the selected counter.

Mode	M2	M1	M0
0	0	0	0
1	0	0	1
2	X	1	0
3	X	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (BCD = 0) or BCD (BCD = 1).

Reading and Loading the Counters

If you attempt to read the counters on the fly when there is a high input frequency, you will most likely get erroneous data. This is partly caused by carries rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it is possible that carries will be propagated from the low to the high byte during the read cycle.

To circumvent these problems, you can perform a counter-latch operation in advance of the read cycle. To do this, load the RW1 and RW2 bits with zeroes. This instantly latches the count of the selected counter (selected via the SC1 and SC0 bits) in a 16-bit hold register. (An alternative method of latching counter(s) that has an additional advantage of operating simultaneously on several counters is through a readback command to be discussed later.) A subsequent read operation on the selected counter returns the held value. Latching is the best way to read a counter on the fly without disturbing the counting process. You can only rely on directly read counter data if the counting process is suspended while reading by bringing the gate low.

For each counter you must specify in advance the type of read or write operation that you intend to perform. You have a choice of loading/reading (a) the high byte of the count, or (b) the low byte of the count, or (c) the low byte followed by the high byte. This last is most generally used and is selected for each counter by setting the RW1 and RW0 bits to ones. Subsequent read/load operations must be performed in pairs in this sequence or the sequencing flip-flop in the 8254 chip will get out of step. The readback command byte format is:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	CNT	STA	C2	C1	C0	0

CNT: When 0, latches the counters selected by bits C0-C2.
STA: When 0, returns the status byte of counters selected by C0-C2.
C0, C1, C2: When high, select a particular counter for readback.
C0 selects Counter 0, C1 selects Counter 1, and C2 selects Counter 2.

You can perform two types of operations with the readback command. When CNT=0, the counters selected by C2 through C0 are latched simultaneously. When STA=0, the counter status byte is read when the counter I/O location is accessed. The counter status byte provides information about the current output state of the selected counter and its configuration. The status byte returned if STA=0 is:

B7	B6	B5	B4	B3	B2	B1	B0
OUT	NC	RW1	RW2	M2	M1	M0	BCD

OUT: Current state of counter output pin.
NC: Null count. This indicates when the last count loaded into the counter register has been loaded into the actual counter. The exact time of load depends on the configuration selected. Until the count is loaded into the counter, it cannot be read.

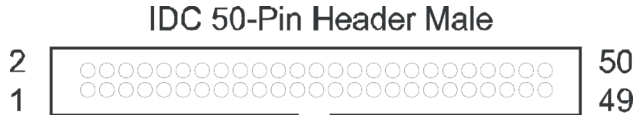
RW1, RW0: Read/Write command.
M2, M1, M0: Counter mode.
BCD: BCD = 0 is binary mode, otherwise counter is in BCD mode.

If both STA and CNT bits in the readback command byte are set low and the RW1 and RW0 bits have both been previously set high in the counter control register (thus selecting two-byte reads), then reading a selected counter address location will yield:

1st Read: Status byte
2nd Read: Low byte of latched data
3rd Read: High byte of latched data

After any latching operation on a counter, the contents of its hold register must be read before any subsequent latches of that counter will have any effect. If a status latch command is issued before the hold register is read, then the first read will read the status, not the latched value.

Chapter 6: Connector Pin Assignments



The PCIe-DIO-24HC card has a 50-pin male connector provided on the back plate of these cards for I/O connections. The mating connector is an TE Connectivity AMP type 1-1658621-0 or equivalent. Connector pin assignments are listed below.

Assignment		Pin
Port C Hi	PC7	1
	PC6	3
	PC5	5
	PC4	7
Port C Lo	PC3	9
	PC2	11
	PC1	13
	PC0	15
Port B	PB7	17
	PB6	19
	PB5	21
	PB4	23
	PB3	25
	PB2	27
	PB1	29
	PB0	31
Port A	PA7	33
	PA6	35
	PA5	37
	PA4	39
	PA3	41
	PA2	43
	PA1	45
	PA0	47
Fused VCCIO		49

Pin	Assignment
2	Counter A0 Input
4	Counter A1 Gate Input
6	Counter A2 Frequency Out
8	Counter B0 Input
10	Counter B1 Gate Input
12	Counter B2 Frequency Out
14	Counter C0 Input
16	Counter C1 Gate Input
18	Counter C2 Frequency Out
20	Digital Interrupt Disable
22	External Interrupt Source
24	Even pins 24-50 are all Ground
26	
28	
30	
32	
34	
36	
38	
40	
42	
44	
46	
48	
50	

Table 6-1: 50-Pin Connector Pin Assignments

Chapter 7: Specifications

Digital I/O

Lines	24; Ports A, B, and C
Type	8255 compatible
Logic Level	VCCIO jumper selectable
Pull-up/down	10k ohm, jumper selectable

VCCIO

Logic Levels	**5V**	
Low Inputs	≤ 1.5V	≤ 2uA
High Inputs	≥ 3.5V	≤ 2uA
Low Outputs	≤ 0.55V	32mA
High Outputs	≥ 3.8V	32mA
Logic Levels	**3.3V**	
Low Inputs	≤ 0.8V	≤ 2uA
High Inputs	≥ 2.0V	≤ 2uA
Low Outputs	≤ 0.55V	24mA
High Outputs	≥ 2.4V	24mA

Counter / Timers

Number / Type	Three 82C54 programmable counters
Counter size	16-bit
Logic level	VCCIO
On-board clock	1MHz
Clock Pulse Width	See 82C54A datasheet

Environmental

Operating Temp.	0° to 70°C, optional -40° to 85°C
Storage Temp.	-55° to +150°C
Humidity	5% to 95% RH, w/o condensation
Dimensions	Length – 4.824"; Height - 4.2" seated

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

ACCES I/O PRODUCTS, INC.
10623 Roselle Street, San Diego CA 92121
Tel. (858)550-9559 FAX (858)550-7322
www.accesio.com